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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/811,113	03/26/2004	Colin Scott Ramsay	W0583.70014 US00	9227

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EXAMINER	
KO, DANIEL BOKMIN	

ART UNIT	PAPER NUMBER
2189	

DATE MAILED: 08/10/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/811,113	RAMSAY ET AL.	
	Examiner	Art Unit	
	Daniel B. Ko	2189	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *26 March 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-26* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-26* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *26 March 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

This action is responsive to the application filed on 3/26/2004. Claims 1-26 have been submitted for examination.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

1. Claims 1, 3-5, 7, 10-14, 20-22, and 25-26 are rejected under 35 U.S.C. 102(e) as being anticipated by Brown et al. (US Patent 6,879,139 B2), hereinafter simply Brown.

Regarding claim 1, Brown teaches a controller comprising:

a logic core having a plurality of inputs and a plurality of outputs (Fig. 1, PRIMARY CONTROL UNIT 11 and SECONDARY CONTROL UNIT 12; column 4, lines 24-67); and

a memory (column 2, lines 55-58);

wherein the controller functions as a state machine and upon the transition from a state to a succeeding state the operation of the logic core (column 5, lines 13-24)

is modified in accordance with data held in the memory (column 3, lines 60-67; column 5, lines 54-67).

Regarding claim 3, Brown teaches a controller, in which the logic core includes a fault detector (column 3, lines 41-52).

Regarding claim 11, Brown teaches a controller in which the logic core comprises a sequence detector (column 3, lines 41-52).

Regarding claims 4 and 12, Brown teaches a controller, in which the fault detector has a plurality of inputs and a lesser number of outputs (column 4, lines 38-52).

Regarding claims 5 and 13, Brown teaches a controller, in which the fault detector has a single output (column 2, lines 27-34).

Regarding claim 7, Brown teaches a controller, in which at least one input detector has multiple signal inputs (column 4, lines 24-67) and it is responsive to the order in which the signal inputs change (column 1, lines 46-57).

Regarding claim 10, Brown teaches a controller, in which the logic core includes a combinational logic unit having a plurality on inputs and a single output, and

wherein at least one of the inputs is selectively maskable and invertable such that the combinational logic unit can be arranged to look for the occurrence of a plurality of input signals being in a predetermined state, and to assert a first predetermined output signal when the input signals are in the predetermined state and a second predetermined output signal when the input signals are not in the predetermined state (column 2, lines 35-50).

Regarding claim 14, Brown teaches a controller, in which the sequence detector comprises a multiplexer responsive to a selection control word to select only one of the plurality of inputs (column 12, lines 5-9).

Regarding claims 20 and 21, Brown teaches a controller in which the memory is user programmable (column 3, lines 53-67).

Regarding claim 22, Brown teaches a controller, in which the memory is non-volatile (column 2, lines 55-58).

Regarding claim 25, Brown teaches a power supply controller (column 3, lines 53-59).

Regarding claim 26, Brown teaches an integrated circuit including a controller (column 5, lines 10-13).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

2. Claims 2, 6, 9, 8, 15-19 and 23-24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Brown et al. (US Patent 6,879,139 B2), hereinafter simply Brown, in view of MacSorley et al. (US Patent 3,626,427), hereinafter simply MacSorley.

Regarding claims 6 and 23, Brown teaches a controller, in which at least one input of the fault detector is associated with a respective input detector which is responsive to at least one of: a mask/select control signal for determining whether an input signal at a signal input of the input detector should be taken into consideration by the fault detector (column 3, lines 53-67).

Brown fails to teach an invert signal for causing an output signal from the input detector to be inverted with respect to the input signal. MacSorley teaches an invert signal for causing an output signal from the input detector to be inverted with respect to the input signal (column 28, lines 35-50; column 48, lines 68-75). At the time of invention it would have been obvious to a person of ordinary skill in the art to combine the Brown with MacSorley. The motivation for doing so would have been a protection of the storage by storage protection circuitry and address the unreachable portion of storage (column 335, lines 74-75; column 336, lines 1-10).

Regarding claim 2, Brown and MacSorely teach a controller, in which the logic core represents a state having up to three outputs (See Brown, column 4, lines 24-67, it is clear that outputs can be up to three).

Regarding claim 8, Brown and MacSorley teaches a controller, in which the fault detector includes combinational logic for combining its inputs in a logical OR (See MacSorely, column 48, lines 1-10).

Regarding claims 9 and 15, Brown and MacSorely teach a controller, in which an output of the fault detector is supplied to a device arranged in a first mode to pass the output of the fault detector in a non-inverted state (See MacSorely, column 29, lines 60-64) and in a second mode to invert the output of the fault detector (See MacSorely, column 28, lines 35-50; column 48, lines 68-75).

Regarding claims 16 and 17, Brown and MacSorely teach a controller in which the sequence detector further includes a sequence timer arranged to assert an output signal only when an input condition monitored by the sequence detector has been in a predetermined state for a predetermined period (See MacSorely, column 224, lines 20-26).

Regarding claims 18 and 24, Brown and MacSorely teach a controller as claimed in claim 1, in which the logic core comprises a time out circuit having a time out timer selectively arranged to assert an output a predetermined period after the logic core has entered a state (See MacSorely, column 76, lines 1-8).

Regarding claim 19, Brown and MacSorely teaches a controller, in which the time out timer is programmable (See MacSorely, column 333, lines 25-45).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Daniel B. Ko whose telephone number is 571-272-8194.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Reginald G. Bragdon can be reached on 571-272-4204. The fax phone number for the organization where this application or proceeding is assigned is 703-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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